

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	testing IC signal quality	USPAT	ADJ	OFF	2006/02/18 20:24
L2	0	IC signal quality	USPAT	ADJ	OFF	2006/02/18 20:24
L3	1	integrated circuit signal quality	USPAT	ADJ	OFF	2006/02/18 20:28
L4	13	"614040"	USPAT	OR	OFF	2006/02/18 20:34
L5	0	("signaltestingofintegratedcircuitchips").PN.	USPAT; USOCR	OR	OFF	2006/02/18 20:35
L6	0	signal testing of integrated circuit chips	USPAT	WITH	OFF	2006/02/18 20:36
L7	1187	power and ground bounce	USPAT	WITH	OFF	2006/02/18 21:27
L8	1	"614040"	US-PGPUB	OR	OFF	2006/02/18 21:26
L9	54	(power and ground bounce).ab.	USPAT	WITH	OFF	2006/02/18 21:27
L10	29089	(power and ground bounce).clm.	USPAT	OR	ON	2006/02/18 21:28
L11	14962	(power with ground bounce).clm.	USPAT	OR	ON	2006/02/18 21:28
L12	27	I9 and I11	USPAT	OR	OFF	2006/02/18 21:28

Patent Assignment Abstract of Title

Total Assignments: 1**Application #:** 10614040**Filing Dt:** 07/08/2003**Patent #:** NONE**Issue Dt:****PCT #:** NONE**Publication #:** US20040123205**Pub Dt:** 06/24/2004**Inventors:** I-Ming Lin, Jen-Nan Liu**Title:** Signal testing of integrated circuit chips**Assignment: 1****Reel/Frame:** 014283 / 0911 **Received:** 07/22/2003 **Recorded:** 07/08/2003 **Mailed:** 01/28/2004 **Pages:** 2**Conveyance:** ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).**Assignors:** LIN, I-MING**Exec Dt:** 03/26/2003LIU, JEN NAN**Exec Dt:** 03/26/2003**Assignee:** VIA TECHNOLOGIES, INC.

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Search Results as of: 2/18/2006 9:14:10 P.M.

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Web interface last modified: September 28, 2005

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L5	0	("signaltestingofintegratedcircuitchips").PN.	USPAT; USOCR	OR	OFF	2006/02/18 20:35
L6	0	signal testing of integrated circuit chips	USPAT	WITH	OFF	2006/02/18 20:36
L7	1187	power and ground bounce	USPAT	WITH	OFF	2006/02/18 21:06
L8	1	"614040"	US-PGPUB	OR	OFF	2006/02/18 21:06

*Majority of search
East cost
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etc*

Day : Saturday

Date: 2/18/2006

Time: 21:09:54

PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = LIN

First Name = I-MING

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10055567	6877103	150	01/22/2002	BUS INTERFACE TIMING ADJUSTMENT DEVICE, METHOD AND APPLICATION CHIP	LIN, I-MING
10140994	6859150	150	05/09/2002	APPARATUS FOR READING KEYBOARD-COMMANDS OF A PORTABLE COMPUTER	LIN, I-MING
10194314	Not Issued	95	07/15/2002	SIGNAL COMPENSATION CIRCUIT OF A BUS	LIN, I-MING
10249439	Not Issued	94	04/10/2003	METHOD AND APPARATUS FOR USING A DYNAMIC RANDOM ACCESS MEMORY IN SUBSTITUTION OF A HARD DISK DRIVE	LIN, I-MING
10368945	6947292	150	02/18/2003	PRIMARY FUNCTIONAL CIRCUIT BOARD SUITABLE FOR USE IN VERIFYING CHIP FUNCTION BY ALTERNATIVE MANNER	LIN, I-MING
10392027	6766391	150	03/18/2003	EMBEDDED CONTROL UNIT	LIN, I-MING
10604268	Not Issued	95	07/08/2003	UTILIZING AN ACPI TO MAINTAIN DATA STORED IN A DRAM	LIN, I-MING
10614040	Not Issued	30	07/08/2003	Signal testing of integrated circuit chips	LIN, I-MING
10665294	6963229	150	09/22/2003	CLOCK SKEW INDICATING APPARATUS	LIN, I-MING
10675942	Not Issued	30	10/02/2003	Universal serial bus keyboard control circuitry	LIN, I-MING
10967244	Not Issued	30	10/19/2004	Peel-off nail polish without polish-remover	LIN, I-MING

Inventor Search Completed: No Records to Display.

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Search Another: Inventor	<input type="text" value="LIN"/>	<input type="text" value="I-MING"/>	<input type="button" value="Search"/>

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Inventor Name Search Result

Your Search was:

Last Name = LIU

First Name = JEN-NAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10614040	Not Issued	30	07/08/2003	Signal testing of integrated circuit chips	LIU, JEN-NAN

Inventor Search Completed: No Records to Display.

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Key: IEEE JNL = IEEE Journal or Magazine, IEE JNL = IEE Journal or Magazine, IEEE CNF = IEEE Conference, II CNF = IEE Conference, IEEE STD = IEEE Standard

1. **Test generation for ground bounce in internal logic circuitry**
Yi-Shing Chang; Gupta, S.K.; Breuer, M.A.;
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25-29 April 1999 Page(s):95 - 104
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2. **Ground bounce considerations in DC parametric test generation using boundary scan**
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26-30 April 1998 Page(s):86 - 91
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3. **Catch the ground bounce before it hits your system**
Kurzweil, E.; Lallement, M.; Blanc, R.; Pasquinelli, R.;
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4. **The effect of test system impedance on measurements of ground bounce in printed circuit boards**
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29 April-3 May 2001 Page(s):358 - 366
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6. **Ground bounce study of 304 lead interposer MQFP with on-chip decoupling capacitor test die**
Huang, C.C.; Loh, B.; Wong, F.;
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7. **Analysis of ground bounce in deep sub-micron circuits**
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8. **Switching activity generation with automated BIST synthesis for performance testing of interconnects**
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9. **A multipath channel model for wideband aeronautical telemetry**
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Dupont, E.; Nicolaidis, M.; Rohr, P.;
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16. **Measurement study on simultaneous switching noise**
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